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20 Years of reconfigurable field-effect transistors: From concepts to future applications

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ABSTRACT

The reconfigurable field-effect transistor (RFET), is an electronic device whose conduction mechanism can be reversibly reconfigured between n-type and p-type operation modes. To enable this functionality, those devices do not rely on chemical doping caused by impurities but rather on electrostatic doping, i.e. the generation of mobile carriers via an external potential. This functionality has been first concieved in the early 2000s to reduce the source-drain leakage in ambipolar thin film transistors. Over the years many different concepts have been developed employing different conduction mechanisms as well as channel materials, such as silicon nanowire, carbon nanotubes or two-dimensional layered materials. In addition the focus the research shifted more and more towards the circuit level, bringing the unique device characteristics to fruitation. In this work, we will give an historic expert of the main development phases including thier key-achievements starting from the earlier years reaching untill today. Further, we give an overview of the most interesting circuit properties arising from the device functionality and summarize the broad range of thier potential future applications.

1. Introduction

The reconfigurable field-effect transistor (RFET), is an electronic device whose conduction mechanism can be reversibly reconfigured between n-type and p-type operation modes. To enable this functionality, those devices do not rely on chemical doping caused by impurities but rather on electrostatic doping, i.e. the generation of mobile carriers via an external potential. Depending on the bias, either electrons or holes are injected into a nominally intrinsic semiconductor. Devices based on this concept have been reported under a variety of names, such as polarity control, dually active channels, charge plasma, Schottky barrier biasing or, field-induced drain extension. Regardless of the name, all devices have in common, that they are composed of at least two independently controlled gate electrodes that electrostatically dope the channel. One, the so-called polarity gate (or program gate, PG) controls the kind of carrier or transport mode, while the control gate (CG) switches the transistor on and off (Fig. 1). The programming thereby can be done statically or dynamically at runtime. In comparison, a classical FET is fixed to either n-type or p-type operation by the underlying fabrication process. This transistor-level reconfigurability has the potential to overcome some of the fundamental limitations of conventional CMOS technologies. The functionality of two devices combined into one leads to a higher level of logic expressiveness, which reduces the costs per basic implemented logic unit. This way reconfigurable transistors can serve as an add-on functionality to increase the versatility of electronics systems without the need for additional scaling. In this work, we will review the history of the last 20 years of RFET development as well as summarize the broad range of their potential future applications.

2. History

2.1. Early phase (2000–2008)

The roots of RFETs go back to the early 2000s when researchers from Taiwan's National Nano Device Laboratories and Institute of Electronics, National Chiao Tung University searched for a way to suppress the undesired high off-state currents in ambipolar Schotty Barrier Thin

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Film Transistors (TFTs). The solution they came up with was to create a device with two gates [1]: one, the control gate, is placed to directly gate the source-sided Schottky junction. This gate and the drain-sided Schottky junction are then covered by a thick oxide. On top of this, a sub gate (which today we would call polarity gate) is placed that covers the complete transistor. By this sub-gate, the undesired carrier injection from the drain-side in the off-state could be lowered by more than three orders of magnitude which resulted in on/off current-ratios as high as 10^6. While this first device was based on TFT technology with polycrystalline silicon [2], a later implementation was based on SIMOX wafers with monocrystalline silicon [3]. This device had an improved architecture achieving max–min current ratios up to 10^9 and subthreshold swings down to 61 mV/dec, but still needed a program voltage significantly higher than the operation voltage. Even though these early reconfigurable FETs have been demonstrated for the first time, due to the very special target application the potential of the technology has not been recognized in the scientific community.

The concept was brought back to attention a couple of years later. Due to the continued scaling of device sizes according to Moore's Law, the stable and reliable operation of MOSFETs has been challenged by the nanoscale device dimensions. Doping by incorporation of chemical impurities became increasingly difficult for ultra-scaled technology nodes because of the increasing impact of dopant fluctuations and dopant deactivation in nanoscale channels [4,5]. As opposed to this, devices facilitating electrostatic doping promised potentially ultra-sharp junctions with well-controlled carrier concentration profiles and reduced defect density [6]. A team from IBM T.J. Watson Research Center realized a reconfigurable FET based on a carbon nanotube as channel material, having a single control gate at the top and a polarity gate covering the whole channel from the backside [7]. The program gate voltage is applied simultaneously at both Schottky junctions. Depending on the sign of the applied voltage, the polarity is set by bending the bands in the semiconducting channel region; a positive (negative) voltage allow the injection of electrons (holes) from both contacts into the entire channel. The top control gate modulates an additional thermionic energy barrier in the center of the channel switching the transistor on and off. Since the carriers are already injected through the Schottky barrier when the control gates operate, the device can achieve an ideal slope of 60 mV/dec at room temperature. Interestingly, the same structure can be also employed for a competing concept called ambipolar operation with selective carrier control [8,9]. In this case, the back gate is operated as a control gate injecting both types of carriers into the channel depending on the applied voltage range. Thus the buried control gate provides an ambipolar behavior when used to steer the channel. The polarity gate placed at the top blocks the undesired charge carrier from passing through the whole channel. In 2008 this concept was improved by a team from Infineon around W.M. Weber, by exploiting a $NiSi_2/Si/NiSi_2$ heterostructure with thermally intruded silicide contacts [10]. This way a gate aligning directly at the drain-sided barrier was used to block the un-desired carrier type [11]. The concept typically exhibits a higher subthreshold slope but a lower source-drain leakage. Until today, all Schottky barrier-based RFETs still rely on either of the two programming mechanisms (Fig. 2), or a combination of both. Also note, that there are other reconfigurable device concepts based on band-to-band tunneling, single-electron, or spin transport, which are beyond the scope of this work.

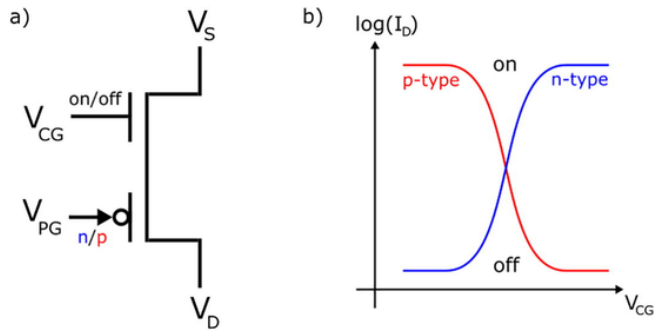

Fig. 1. Schematic representation of RFET operation, a) generic symbol b) generic characteristics. Depending on the applied signal at the polarity gate (PG) either n-type or p-type characteristics are achieved when the device is steered at the control gate (CG).

2.2. Device outgrowth and first logic gates (2009–2013)

Following and improving the two basic mechanisms proposed, research groups have been focused on 1-dimensional nanostructures, predominantly silicon nanowires [12–16] in the following years. The name "Reconfigurable Field Effect Transistor" itself was first introduced by Heinzig et al. from NaMLab in 2012 [12], for an improved demonstrator of the concept with independent control of carrier injection (Fig. 2 (b)). The device was refined just one year later, showing perfect symmetry between n-type and p-type currents [16] which is a prerequisite for the efficient use of reconfigurability in CMOS-like circuits. This was achieved by employing oxidation-induced mechanical stress into the

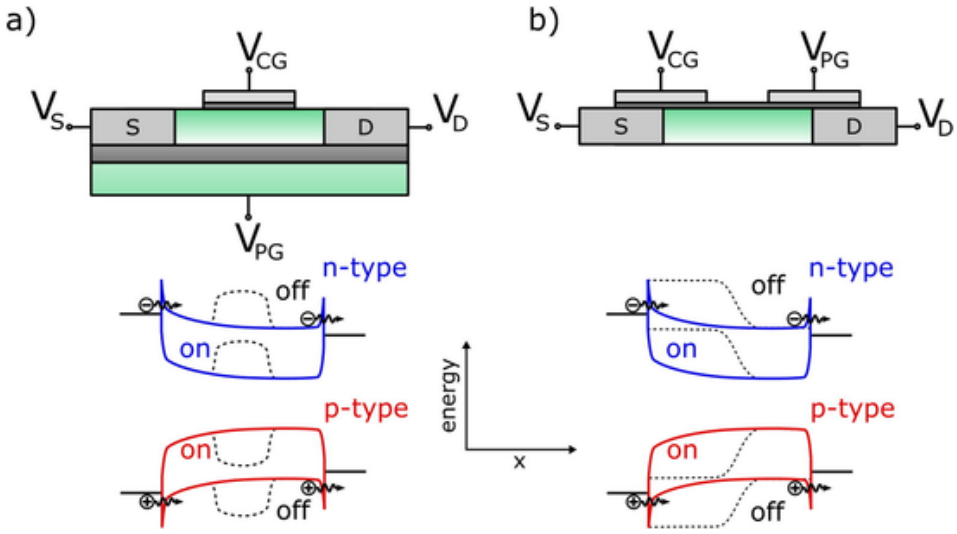

Fig. 2. Main concepts to enable reconfigurability on a Schottky barrier FET. (a) Polarity control at both barriers and transport over a thermionic barrier in the center of the channel. (b) Control of carrier injection directly at the source-sided Schottky junction and blocking of the undesired carrier type at drain.

channel [17], enabling an operation with only two distinctive potentials V_{DD} and ground. The operation was verified by demonstrating the first reconfigurable complementary inverter circuit [16]. In 2012 a research group at EPFL has shown that a three gated device with the two outer gates overlapping the Schottky junctions largely improves the concept of back-gate programming, lowering the programming voltage and simplifying process integration [13].

Simultaneously with these more sophisticated device demonstrators, the development of the first logic gates exploiting the reconfigurability started. In this regard, two major design paradigms can be distinguished in the literature at the logic optimization level to achieve more functionality per computational unit – implicit and explicit reconfigurability [18]. Explicit reconfigurability is realized in those circuits which can alter the functionality by an external signal on request. Here, a simple example is a NAND gate, which can be dynamically reprogrammed to NOR functionality when built from RFETs [19]. In contrast, implicit reconfigurability can be used in logic gates where a particular combination of inputs results in an electrical scenario that yields a truth table with a higher expressive capability. For example, exploiting three-gated RFETs compact realizations of XOR and MAJ can be built using a lower number of transistors than in classical CMOS [13].

2.3. Functional diversification (2014–2020)

After the first demonstration of device and logic gate features research activities went into a rapid growth (Fig. 3). The devices started to diversify in terms of material and transport physics. At first silicon nanowires have been replaced by more industry-oriented platforms, like FinFETs [20] or planar SOI-based FETs [21]. Low-bandgap materials like germanium have been shown to increase the performance and lower the threshold voltages [22]. On the other hand, also 2-dimensional layered systems, like graphene [23], transition-metal dichalcogenides, e.g. WSe_2 [24] or $MoTe_2$ [25,26], and black phosphorous [27] have been put into the focus. Concepts with only one [28], as well as, three [29] or four [30] independent gates have been shown. The concept of polarity-control has been extended to mode control [31], e.g. by exploiting the differences in threshold voltages of three-independent-gate devices. Impact ionization in combination with a positive feedback effect has been demonstrated as an option to yield steep subthreshold slopes down to 6 mV/dec [20]. Also, add-on features like non-volatile storage of the polarity program have been demon-strated [32,33] These features will further enrich the possibilities of circuit designers employing RFETs.

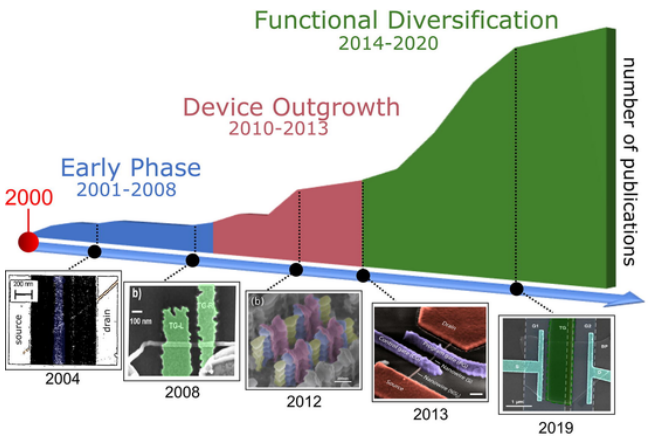

Fig. 3. RFET device development over time. Number of publications represent published RFET device concepts over time as of the internal database of the authors. Key developments are indicated.

3. Towards future applications

Several circuit level features have been demonstrated for RFETs, which provide an added benefit over their CMOS counterparts: dynamic reconfiguration [19,34], intrinsic XOR [35] and wired-AND capabilities [30], control of threshold voltage [29], and suppression of parasitic charge sharing effects in dynamic logic gates [36,37]. Pioneering studies have proven, that this higher expressive capability of RFETs yields an added benefit on the circuit level, rather than the device level itself. In the predictive PDK by Gore et al. [38] 42% of area savings over a 10 nm FinFET process have been predicted for a 1-bit full adder design, despite the larger individual transistor size. Similarly, Raitza et al. [39] have predicted a 25% gain in critical path delay of a 16-bit conditional carry adder by reducing the number of stages and making efficient use of reconfiguration. Reconfigurable transistor concepts have also been proposed for the co-integration of several add-on functionalities into classical CMOS, which goes beyond general computing purposes. The polymorphic nature of RFET circuits enables new approaches on hardware security solutions, such as logic locking, camouflaging, physically unclonable functions (PUFs), or chip authentication [27,40–45]. RFET-based XOR cells and flip-flops are less prone to delay-side-channel attacks than their CMOS counterpart [45]. Beyond that, the reconfigurable nature holds a lot of promises also for analog and mixed-signal designs [46,47], cryo-CMOS [48] as well as new operation schemes, such as asynchronous or neuromorphic computing [43]. One particular path to pursue in this regard is the very efficient XOR and XNOR implementation enabled by the RFET base technology which is suitable for the application in binary neuronal networks [49]. Also, synaptic cells for emulating spike-time-dependent behavior have been proposed [50].

To enable a sufficient circuit design for all of these applications, a crucial aspect is the development of accurate models and overall support of the electronic design automation. Efficient compact models have to be developed reflecting the physics of the device [38,51,52], which is distinctively different than that of classical MOSFETs. Standard cell libraries have to be derived giving credit to the higher expressive capability of the RFET technology [53–56]. At the logic synthesis level, new data structures are needed to yield the full potential of these features [57]. For example, it has been shown that self-dual logic gates based on RFETs are a better choice for standard cells as they are more efficiently implemented with reconfigurable technology [58]. The same is true for the technology mapping stage [18], as well as physical synthesis flows. In 2018 a first complete physical synthesis flow for emerging reconfigurable nano-technologies using open-source tools was made available [55] to foster future circuit design activities.

4. Conclusion

In this work, we have given an overview of the development of reconfigurable field-effect transistors based on electrostatic doping. Key achievements over the past 20 years have been summarized. Finally, a view on potential future applications and development tasks has been presented.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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References

[1] H. C. Lin et al., in International Electron Devices Meeting 2000. Technical Digest. IEDM, Dec. 2000, pp. 857–859
[2] Lin HC, Yeh KL, Huang RG, Lin CY, Huang TY IEEE Electron Device Lett 2001;22(4):179–81.
[3] H. C.Lin, et al., in 60th DRC. Conference Digest Device Research Conference, Jun. 2002, pp. 45–46.
[4] Mikolajick T, Häublein V, Ryssel H Appl Phys A 1997;64(6):555–60.
[5] J. Knoch and M. R. Mueller, IEEE Trans. Nanotechnol., vol. 13(6), 2014
[6] Gupta G, Rajasekharan B, Hueting RJE IEEE Trans Electron Devices 2017;64(8):3044–55.
[7] Y.-M. Lin J. Appenzeller P. Avouris in Electron Devices Meeting, IEDM Technical Digest IEEE International, Dec. 2004 2004 687 690
[8] Koo S-M, Li Q, Edelstein MD, Richter CA, Vogel EM Nano Lett 2005;5(12):2519–23.
[9] Colli A, Tahraoui A, Fasoli A, Kivioja JM, Milne WI, Ferrari AC ACS Nano 2009;3(6):1587–93.
[10] Weber WM, et al. Nano Lett 2006;6(12):2660–6.
[11] W. M. Weber et al., 8th IEEE Conference on Nanotechnology, 2008. NANO '08, pp. 580–581, Aug. 2008
[12] Heinzig A, Slesazeck S, Kreupl F, Mikolajick T, Weber WM Nano Lett 2012;12(1):119–24.
[13] M. De Marchi et al., in Electron Devices Meeting (IEDM), 2012 IEEE International 2012 pp. 8.4.1-8.4.4
[14] Wessely F, Krauss T, Schwalke U Microelectron J 2013;44(12):1072–6.
[15] Mongillo M, Spathis P, Katsaros G, Gentile P, De Franceschi S Nano Lett 2012;12(6):3074ff.
[16] Heinzig A, Mikolajick T, Trommer J, Grimm D, Weber WM Nano Lett 2013;13(9):4176.
[17] Baldauf T, Heinzig A, Trommer J, Mikolajick T, Weber WM Solid-State Electron 2017;128:148.
[18] S. Rai, M. Raitza, and A. Kumar, 2018 Design, Automation Test in Europe Conference Exhibition (DATE), Mar. 2018, pp. 767–772
[19] Trommer J, Heinzig A, Slesazeck S, Mikolajick T, Weber WM IEEE Electron Device Lett 2014;35(1):141–3.
[20] J. Zhang, M. De Marchi, P.-E. Gaillardon, and G. De Micheli, Proc. Int. Electron Devices Meet. IEDM'14, 2014
[21] Krauss T, Wessely F, Schwalke U ECS J Solid State Sci Technol 2015;4(5):Q46–50.
[22] Trommer J, et al. ACS Nano 2017;11(2):1704–11.
[23] S. Nakaharai et al., in Electron Devices Meeting (IEDM), 2012 IEEE International, Dec. 2012, pp. 4.2.1
[24] Resta GV, et al. Sci Rep Jul. 2016;6:29448.
[25] S. Nakaharai, M. Yamamoto, K. Ueno, Y.-F. Lin, S. Li, and K. Tsukagoshi, ACS Nano, vol. 9 no. 6 May 2015,
[26] Larentis S, et al. ACS Nano 2017;11(5):4832–9.
[27] Wu P, Reis D, Hu XS, Appenzeller J Nat Electron 2021;4(1):45–53.
[28] Darbandy G, Claus M, Schröter M IEEE Trans Nanotechnol 2016;15(2):289–94.
[29] J. Zhang, P.-E. Gaillardon, and G. De Micheli, in 2013 IEEE International Symposium on Circuits and Systems (ISCAS), May 2013, pp. 2111–2114
[30] M. Simon et al., in 2018 76th Device Research Conference (DRC), Jun. 2018, pp. 1–2,
[31] P.-E. Gaillardon, J. Zhang, M. De Marchi, and G. De Micheli," 2015 IEEE Nanotechnology Materials and Devices Conference (NMDC). IEEE, 2015.
[32] Park J-M, Bae J-H, Eum J-H, Jin SH, Park B-G, Lee J-H IEEE Electron Device Lett 2017;38(5):564–7.
[33] S. J. Park et al., Adv. Electron. Mater., vol. 4, no. 1, p. 1700399, 2018.
[34] Rai S, Trommer J, Raitza M, Mikolajick T, Weber WM, Kumar A IEEE Trans Very Large Scale Integr VLSI Syst 2019;27(3):560–72.
[35] De Marchi M, et al. IEEE Electron Device Lett 2014;35(8):880–2.
[36] Trommer J, Simon M, Slesazeck S, Weber WM, Mikolajick T IEEE J Electron Devices Soc 2020;8:740–7.
[37] Vana D, Gaillardon P-E, Teman A IEEE Trans Nanotechnol 2020;19:123–36.
[38] G. Gore, P. Cadareanu, E. Giacomin, and P.-E. Gaillardon, in IFIP/IEEE 27th International Conference on Very Large Scale Integration (VLSI-SoC), Oct. 2019
[39] M. Raitza et al., Proc. Des. Autom. Test Eur., 2017.
[40] Y. Bi et al., J Emerg Technol Comput Syst, vol. 13, no. 1, pp. 3:1–3:19, Apr. 2016.
[41] Y. Bi, K. Shamsi, J.-S. Yuan, F.-X. Standaert, and Y. Jin, in 2016 Design, Automation & Test in Europe Conference & Exhibition (DATE), 2016, pp. 1538–1543, 2016.
[42] J. Knechtel, Proc. 2020 Int. Symp. Phys. Des., vol. 2020, pp. 75–86, Jan. 2020.
[43] S. Rai, S. Patnaik, A. Rupani, J. Knechtel, O. Sinanoglu, and A. Kumar, IEEE Trans. Emerg. Top. Comput., pp. 1–1, 2020.
[44] A. Rupani, S. Rai, and A. Kumar, in 2019 22nd Euromicro Conference on Digital System Design (DSD), Aug. 2019, pp. 668–671.
[45] E. Giacomin and P.-E. Gaillardon, in 2018 IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC), Oct. 2018, pp. 107–112.
[46] Harada N, Yagi K, Sato S, Yokoyama N Appl Phys Lett 2010;96(1):012102.
[47] P. E. Gaillardon, M. Hasan, A. Saha, L. Amarú, R. Walker, and B. S. Rodriguez, in 2016 IEEE International Symposium on Circuits and Systems (ISCAS), May 2016, pp. 405–408.
[48] Zhang J, Trommer J, Weber WM, Gaillardon P-E, De Micheli G Electron Devices Soc IEEE J 2015;3(6):452–6.
[49] Bae J, et al. IEEE Electron Device Lett 2019;40(4):624–7.
[50] C. Pan et al., Nat. Electron., vol. 3, no. 7, pp. 3832020.
[51] M. Hasan, P. Gaillardon, and B. Sensale-Rodriguez IEEE J. Electron Devices Soc.,vol. 5, no. 1, pp. 23–31, 2017.
[52] Ni W, Dong Z, Huang B, Zhang Y, Chen Z IEEE Access 2021;9:46709–16.
[53] Reuter M, Pfau J, Krauss TA, Becker J, Hofmann K IEEE Trans Circuits Syst Regul Pap 2021;68(1):114–25.
[54] J. Nevoral, R. Růžička, and V. Šimek, in 2018 21st Euromicro Conference on Digital System Design (DSD), Aug. 2018, pp. 657–664.
[55] S. Rai et al., in 2018 Design, Automation Test in Eu-rope Conference Exhibition (DATE), Mar. 2018, pp. 605f.
[56] Raitza M, et al. IEEE Access 2020;8:112598.
[57] L. Amarú, P.-E. Gaillardon, and G. De Micheli, IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst., vol. 35, no. 5, pp. 806–819, May 2016.
[58] S. Rai, M. Raitza, S. S. Sahoo, and A. Kumar, in Proc. Des. Autom. Test Eur., 2020.

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